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Intellectual Property Administration  
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MAY 27 2003

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P A T E N T & T R A D E M A R K O F F I C E

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Osamu S. Nakagawa

Confirmation No.: 3635

Serial No.: 09/891,324

Examiner: Schillinger, Laura M.

Filed: June 27, 2001

Group Art Unit: 2813

Title: PROCESS FOR HIGH-DIELECTRIC CONSTANT METAL-INSULATOR  
METAL CAPACITOR IN VLSI MULTI-LEVEL METALIZATION SYSTEMS

MAIL STOP AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

6/13/03  
Sir:

In response to the Official Action dated March 27, 2003, kindly amend the application identified above in the following manner:

IN THE SPECIFICATION:

*Please amend the specification by replacing the paragraph beginning on page 8, line 21 and ending on page 9, line two, with the following paragraph:*

Returning to Fig. 2, in step 235, a second layer of metal 350 is deposited on top of the patterned interlevel dielectric layer 335 (see Fig. 3E) to form the signal via 355 and the electrode vias 340-344, and an upper electrode 360 of a high-k constant MIM capacitor 370. The second layer of metal is finished by a second CMP process to complete the vias 338-344 and upper electrode 360, in step 240.

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